High-Speed Measurements Need Record Length To Match

One of the realities of today's high-speed serial bus compliance and validation work is a much-increased requirement for analysis of acquired signals. Eye diagrams, jitter analysis, modulation and clock measurements, and various signal quality metrics all influence the technical demands made on the oscilloscope. A high-performance oscilloscope must not only acquire, but also store for analysis (detailed signal data gathered at high sample rates). Equally important, the amount of time that must be recorded — as expressed in clock cycles, pattern bits, or unit intervals — is also on the increase. An oscilloscope that lacks sufficient record length may be unable to deliver results accurately, efficiently…or at all.

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Enabling Innovation

Sample Rate, Time, and Record Length

Behind the front panel, underlying digital storage oscilloscope (DSO) architecture includes an acquisition system (including triggering), a display system, and a memory. This memory stores the sample points that accumulate in the course of an acquisition. The memory is of course finite; today's highest-bandwidth oscilloscopes offer memory depths ranging from 250K (250,000 points) to 64M (64 million points).

Proprietary architectural choices determine the ultimate size of the memory. Some oscilloscope systems integrate key high-speed elements such as the A/D, demultiplexer, and memory on a single chip. This approach limits the depth of the high-speed memory, since chip real estate must be shared among so many functions. Instruments using this architecture supplement the small high-speed memory with slower "external" memory that cannot store data at the maximum sample rate.

An alternative approach is to integrate the oscilloscope's "front end" using the fastest available semiconductor technologies, particularly Silicon Germanium (SiGe), and use a dedicated high-speed sample memory. This architecture can support the oscilloscope's full sample rate, bandwidth, and record length all at once, and the sample memory is not constrained by silicon real-estate considerations. The Tektronix TDS6000C Series relies on this configuration, providing memory depths to 64M, accessible at the instruments' full 40 GS/s sample rate.

The memory records events that occurred over a span of time, so in practical terms it is storing "time". When acquiring a signal with a DSO, sample rate and stored time have an inversely proportional relationship. It makes sense: as you increase the sample rate (take samples more frequently), the memory fills up faster. And the guidelines of the Nyquist Theorem require you to increase the sample rate as the frequency of the measured signal increases[*1] .

For the sake of discussion, let's imagine a memory with a capacity of 1,000,000 (1M) points—smaller than most laboratory oscilloscopes, but sufficient to illustrate the concept. If you acquire a 50 kHz signal at a rate of 100,000 samples per second, the memory will fill in 10 seconds.

Next, suppose you raise the sample rate to 1,000,000 samples—one megasample—per second (1 MS/s). This is enough to correctly acquire a signal with a frequency of 500 kHz. At this new sample rate, the memory fills up in just 1 second.

Now multiply the original sampling frequency by a factor of 40,000. The sample rate becomes 40 gigasamples per second, the range needed to address today's fastest serial transmission standards. Imagine what happens to the time represented by that 1M memory! It can store all of 25 microseconds' worth of signal data, irrespective of the signal frequency being observed.

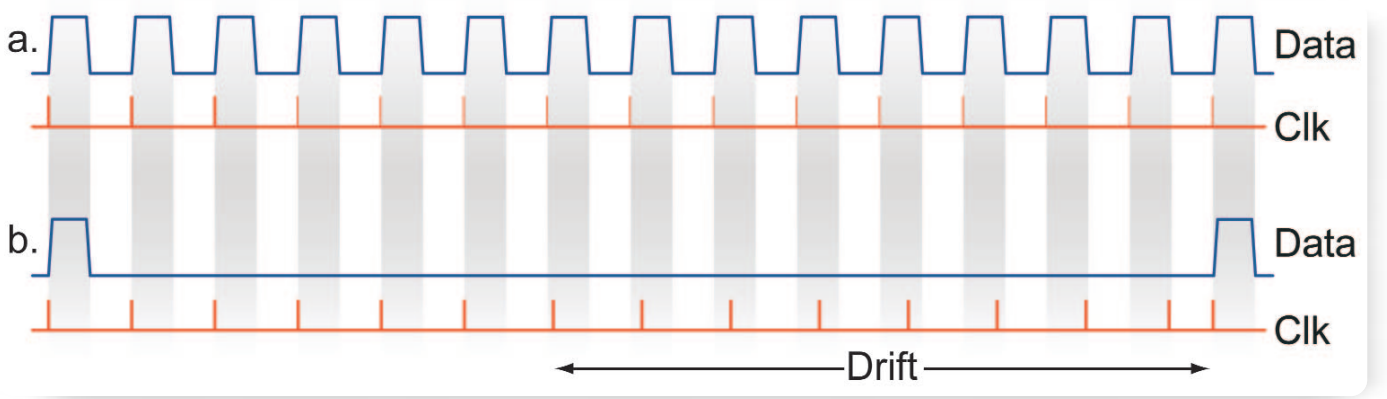
Pseudo-Random Bit Streams Challenge Oscilloscopes' Speed And Depth

Rigorous validation and troubleshooting measurement for devices employing serial bus technologies such as SATA II and PCI Express depend on the ability to store long data patterns. And that translates directly to a requirement for ample memory depth.

A case in point is the PRBS2^x-1 pattern. This pseudo-random bit stream (PRBS) tool essentially cycles through a complete sequence of binary values, where the total count can be any practical power of two, from 2^7 through 2^{31}. The PRBS2^7-1 is sometimes used when short patterns are adequate to mimic the range of values encountered in 8b/10b encoding.

The PRBS2^7-1pattern is sometimes cited to demonstrate an oscilloscope's ability to acquire and analyze demanding digital patterns. But with a mere 127 bits (1016 stored sample points) taken at 20 GS/s, the PRBS2^7-1 pattern demands very little of the oscilloscope's memory.

[*1]The Nyquist Theorem states that the sample rate must be at least twice that of signal being sampled in order to avoid aliasing, a form of distortion.



▸ **Figure 1.** *Differing states of the PRBS23-1 pattern can have differing effects on the clock. Waveform (a) changes states in every unit interval, keeping the embedded clock synchronized. Waveform (b) is a worst-case situation with many consecutive identical digits that can tend to let the clock drift. A full PRBS23-1 acquisition will capture these states and all others, and help identify resulting errors.*

The PRBS23-1 pattern delivers a practical range of values for high-speed serial elements conforming to standards such as SONET and 10 Gigabit Ethernet, and for uncompressed digital video. The sequence encompasses 8,388,607 binary values, which equates to 2^{23} minus one. The PRBS23-1 pattern's demands on the device under test approximate the effects of random data in a complex system.

Comprehensive NRZ (Non-Return To Zero) patterns include long sequences of consecutive identical digits (CID) which act like low-frequency components in the signal. Although there are shortcuts that rely on a smaller number of "more stressful" binary states to test worst-case behavior, there is no substitute for an exercise that runs through all possible binary combinations of the data word. This is exactly what the PRBS23-1 pattern does. The pattern has been recommended by digital device vendors[*2] as a good representation of random NRZ data.

The PRBS23-1 pattern is particularly good at exposing an embedded clock's tendency to drift. Clock drift can be a source of jitter, and jitter occurring anywhere in a digital system can have a degrading impact on timing tolerances throughout.

Traces "a" and "b" in Figure 1 depict the situation. The two waveforms represent two of the many binary states (not all bits are shown) that occur in the execution of a PRBS23-1 pattern. Trace "a" is a best-case situation with alternating 1 and 0 values. There are no consecutive identical digits. Every unit interval includes a transition that acts as a timing reference for the embedded clock signal.

Trace "b" in Figure 1 symbolizes a value with the maximum number of CID bits (zeroes in this case) bounded by a "one" bit on each end. Clearly this pattern word will not refresh the embedded clock regularly. The long string of unchanged data provides no reference edges to synchronize with. It is all too easy for the clock to drift a slight amount during this cycle. Over the course of thousands of cycles, this drift appears as time interval error or jitter.

The PRBS23-1 pattern drives the need for an oscilloscope with memory capacity enough to store this large amount of data. Capturing and storing the entire sequence on each trigger ensures that all possible data combinations are observed. Anything less leaves some combinations unseen, potentially allowing erratic time interval errors to pass undetected.

Of course, it is important to remember that each data bit in the pattern requires several samples to capture the waveform; that is, a stored sample is not the same thing as a "bit" in the digital word.

[*2] "Spectrum content of NRZ test patterns," Justin Redd and Craig Lyon, (Maxim Integrated Circuits); EDN magazine, September 2, 2004

Like all other sampling applications, the sampling frequency must be at least twice that of the fundamental frequency being measured. Fortunately, oscilloscopes with sample rates of 20 GS/s are suitable for emerging serial technologies in the 2.5 Gb/s, 3.125 Gb/s, and 5.0 Gb/s ranges, while the latest 40 GS/s instruments can handle foreseen requirements for 6.0 Gb/s and above. Consider these memory requirements when running the maximum sample rate:

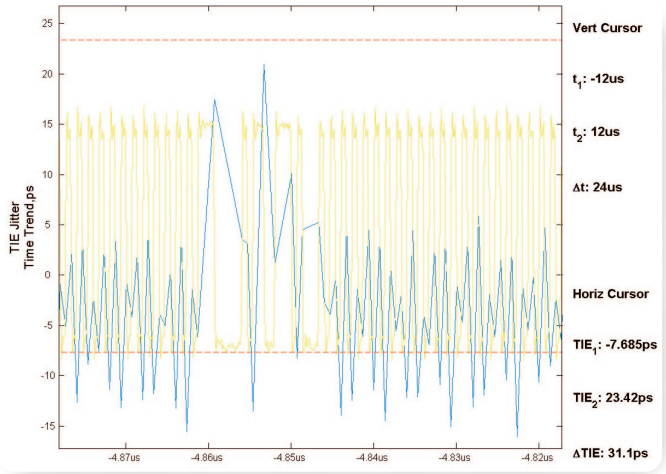
– A PRBS23-1 pattern running at 3.0 Gb/s delivers a total of 8,388,607 bits in approximately 2.83 ms. When sampling at 20 GS/s, the oscilloscope stores 56.8 million sample points to represent the data.

– A PRBS23-1 pattern running at 6.0 Gb/s delivers a total of 8,388,607 bits in 1.41 ms. The oscilloscope needs to sample at 40 GS/s for maximum waveform resolution. In doing so, it stores 56.8 million sample points to represent the data.

There is no substitute for adequate record length. A memory depth of, say, 2M points can store only about 3% of the PRBS23-1 pattern—hardly enough to make an informed evaluation of the device's response to the stimulus.

Attempting to capture the PBRS23-1 pattern with multiple acquisitions is at best a tricky and uncertain proposition. An edge trigger will never occur during a sequence of CIDs, since by definition there are no edge transitions to cause a trigger. Even with multiple acquisitions some patterns will be consistently ignored.

Figure 2 is a Time Interval Error (TIE) plot of a serial data waveform. The yellow trace is the actual data. The TIE jitter appears in blue. TIE jitter is a measure of edge jitter compared to a reference, in this case the data clock. The measurement reveals clock drift and pattern-dependent jitter.



▶ **Figure 2.** *A Time Interval Error plot of a serial data waveform. The blue trace indicates clock drift and pattern-dependent jitter in the signal.*

Note that the maximum TIE in this plot correlates closely with certain patterns. The errors derive not only from the number of consecutive identical digits, but also the specific pattern. This confirms the importance of testing all possible data combinations, which is exactly what the PRBS23-1 pattern does. And the PRBS23-1 pattern, as we have seen, requires a very long record length to capture all the necessary data.

One more detail impacts memory use. Commonly the embedded clock is recovered as part of process executed by software such as Tektronix TDSRT-Eye™. The software emulates the action of a Phase Lock Loop (PLL) with variable frequency response. The algorithm requires a number of cycles to lock on the data, and this consumes record length. The amount of memory required for PLL lockup depends on the data rate, the time constant of the PLL, and the particular pattern of data preceding the trigger point.

Memory consumed by the software clock recovery is not available for waveform capture. If the clock recovery takes 5 microseconds (a common value in 2.5 Gb/s standards) and the total record length is only 12.5 microseconds, then the capacity for actual waveform data is severely constrained.

Spread Spectrum Clocks — "Slow" And Fast At The Same Time

Long record length is also a valuable asset for measuring low-frequency events such as spread spectrum clock (SSC) modulation. Without sufficient high-speed memory depth, it is not possible to capture even one full modulation cycle of a typical SSC clock implementation.

Serial ATA specifications, for example, define an SSC modulation frequency of 30 kHz to 33 kHz. Obviously this is an entirely different scale than that of the data itself, which runs at multi-gigabit data rates. Consider these requirements spelled out in the SATA standard, also applicable to SATA II:

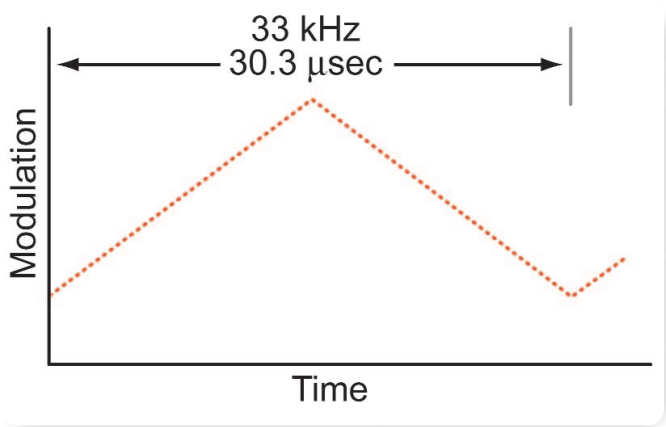
– When SSC is employed, all device timings (including jitter, skew, clock period, output rise/fall times, etc.) must meet the existing non-SSC specifications

– The minimum Unit Interval (UI) time is 666.43 ps for the active data signal; the maximum is 670.12 ps

– The preferred modulation method is "down-spreading;" adjusting the spread technique to preclude modulation above the nominal frequency.

– For triangular modulation, the clock frequency deviation must be down-spread and shifted no more than 0.5% from the nominal frequency; that is, +0%/-0.5%.

– The modulation frequency of the SSC must be in the range of 30 to 33 KHz



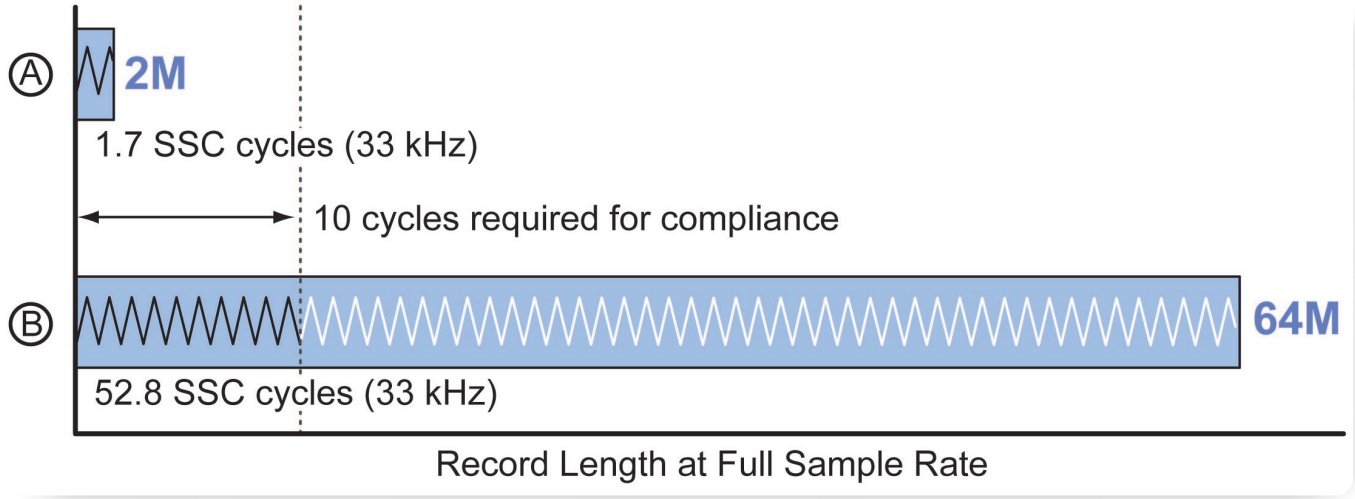
▸ **Figure 3.** *Spead-spectrum clock modulation profile as presented in the SATA 1.0a specification; also applicable to SATA II.*

Figure 3 illustrates the SSC modulation profile for a SATA or SATA II device. When the modulation envelope goes more positive, the clock period gets longer with each successive cycle (UI). At the peak of the modulation envelope, the period is at its longest, then it begins to decrease in step with the modulation profile.

Note again the requirement that limits SSC modulation to no more than .5% from the nominal frequency. This small amount of modulation is virtually impossible to observe in real time with a conventional oscilloscope measurement. To analyze the behavior of an SSC-modulated signal, it is necessary to capture and store at least ten cycles' worth of modulation activity, recover the embedded clock, then plot the change in the clock period over time. A tool such as the TDSJIT3 v2.0, jitter measurement package[*3] is indispensable for this analysis job.

To faithfully capture the data, the oscilloscope must acquire at an appropriate sample rate; 40 GS/s in the case of the fastest serial protocols. Yet it also must store enough "time" to accumulate ten cycles of a 30.3 microsecond modulation envelope.

[*3]TDSJIT3 is a high-resolution automated jitter measurement tool whose versatility allows it to track low-frequency SSC modulation. Importantly, true jitter measurements also benefit from long record length. Jitter is a statistical entity. Because since more "time" can be stored, the statistical analyses can draw from a larger population of samples, increasing the accuracy of the measurement.



▸ **Figure 4.** *Spread spectrum clock (SSC) measurements require both deep memory and high speed: at least 10 cycles of the SSC modulation envelope at full sample rate. Here the difference between a 2M memory ("A") and a 64M memory ("B") is shown to scale. The 64M record length has more than enough capacity for the required 10 cycles of SSC modulation.*

$$\text{Modulation Envelope duration} \over \text{Sample Interval @ 40 GS/s} \quad \frac{30.3 \times 10^{-6}}{2.5 \times 10^{-11}} \times 10 = 12{,}120{,}000 \text{ sample points}$$

Quickly calculating the necessary capacity, we divide the 30.3 microsecond envelope by the sample interval at 40 GS/s, namely 25 ps (2.5 x 10^{-11} seconds), to yield the amount of memory required to store one cycle; then multiply that result by 10.

The sample memory required to store the minimum ten cycles is just over 12M points. Should there be a need to store even more data, oscilloscopes such as the TDS6804C can be equipped with up to 64M memory depth; enough for more than 50 cycles of SSC modulation.

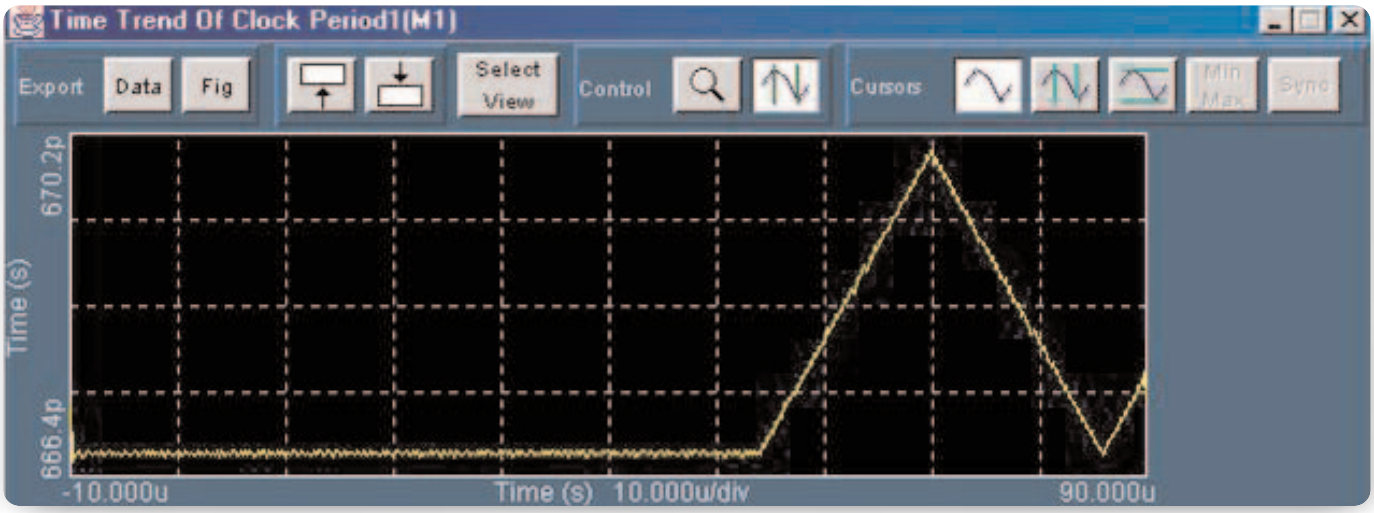
Figure 4 compares the storage capacity of two memory configurations. Both are capable of recording data at a 40 GS/s sample rate. Instrument "A" uses on a small local (2M) memory for high speed storage. While there is additional record length available, this supplementary storage cannot record at the full 40 GS/s.

In contrast, instrument "B" offers maximum record length—64M points—combined with maximum sample rate. As the graph indicates, this configuration provides ample space to store data over the requisite 10 cycles of SSC clock modulation, and more.

Once the signal data is stored, the TDSJIT3 analysis application can establish a reference clock from the data signal and automatically plot the changes in the recovered clock period.

Figure 5 depicts a TDSJIT3 record showing the SSC clock modulation profile observed on an SATA bus. The plot shows frequency deviation in the signal mapped over the allowable range of unit interval tolerances. The baseline value is the minimum UI: 666.4 ps. The peak excursion approaches—but does not exceed—the maximum UI, that is, 670.1 ps. The period of the 1.5 GHz clock is changing by less than 4ps.

Thanks to the deep memory available at full sample rate, we have information to prove that the modulation profile complies with the published standard.



▸ **Figure 5.** *Modulation profile for a spread-spectrum clock. Capturing the necessary 10 cycles of modulation for compliance testing requires more than 12M of sample memory.*

Long-Term Record Length Has Many Applications

The value of a deep sample memory is not confined to a few specialized applications. It is useful in everyday troubleshooting work, and in a host of key compliance tests.

Deliberate low-frequency modulation such as SSC is not the only long-wavelength phenomenon that confronts designers. Unintended trends such as power supply fluctuations can cause, for example, an embedded clock to drift erratically from its assigned frequency. Such events may only be visible amid long-term accumulations of data, often acquired at maximum sample rate. A sample memory that is too small for the application imposes an unacceptable low-frequency "boundary" on any acquisitions – approximately 20 kHz when a 2M memory is filled with samples at 40 GS/s. At frequencies below this boundary, it is not possible to store an entire cycle's worth of samples. This may make it impossible to troubleshoot ordinary frequency drift problems in an emerging digital design.

Compliance tests for some serial transmission standards require acquisition of a specific number of consecutive unit intervals; just a few hundred in some cases, thousands of unit intervals in others; and in general the required number of UI is increasing. Clearly this is another example that highlights the importance of uncompromised record length at full sample rate.

Summary

Today's exacting high-speed measurements demand more than just oscilloscope bandwidth; they call for a deep memory to store the results of acquisitions at sample rates up to 40 GS/s. Some applications require storing tens of millions of samples to characterize jitter behavior and pattern sensitivity. Others call for accumulating long-term trends such as clock modulation or frequency drift.

While some solutions split the memory into higher- and lower-speed elements to achieve great depth, ultimately there is no substitute for uncompromised full-bandwidth storage.

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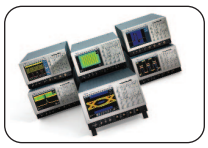

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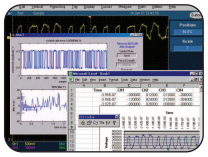

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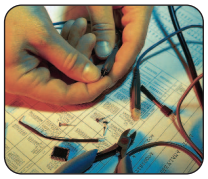

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